Amendments to the Specification:

Please replace paragraph **[0006]** with the following amended paragraph:

[0006] Increasing circuit density has not only improved the complexity and performance of ICs but has also provided lower cost parts to the consumer. An IC fabrication facility can cost hundreds of millions, or even billions, of dollars. Each fabrication facility will have a certain throughput of wafers, and each wafer will have a certain number of ICs on it. Therefore, by making the individual devices of an IC smaller, more devices may be fabricated on each wafer, thus increasing the output of the fabrication facility. Making devices smaller is very challenging, as each process used in IC fabrication has a limit. That is to say, a given process typically only works down to a certain feature size, and then either the process or the device layout needs to be changed. An example of such a limit is the ability to form interchanging metal and dielectric layers, where the metal layers ~~to~~ do not interact with each other in the form of noise.

Please replace paragraph **[0010]** with the following amended paragraph:

[0010] In a specific embodiment, the invention provides a method for manufacturing integrated circuit devices including capacitor structures, e.g., ~~metal-insulator-metal~~ a metal-insulator-metal. The method includes providing a substrate including an overlying thickness of a first insulating material. The substrate is a semiconductor wafer, such as a silicon wafer or the like. The method includes forming a plurality of openings within the thickness of the first insulating material and a region of the dielectric material. Each of the openings includes a width and a height. The method includes forming a barrier layer overlying an exposed surface of each of the plurality of openings. Each of the openings is filled with a metal layer, which ~~occupying~~ occupies substantially an entire region of each of the openings to form a plurality of metal structures. Each of the metal ~~structure~~ structures has a width and a height. The method also planarizes a surface of the metal layer. The method also includes patterning the region to expose each of the metal structures to expose the barrier layer overlying each of the metal structures. A capacitor dielectric layer is formed overlying each of the exposed barrier layer structures. The method also includes forming a second metal layer overlying the capacitor dielectric layer overlying the barrier layer structures. Each of the metal layer structures overlying the capacitor

~~insulating~~ dielectric layer, and the second metal layer form~~s~~ a capacitor structure. The method planarizes the second metal layer.

Please replace paragraph **[0021]** with the following amended paragraph:

[0021] Figures 1 through 6 illustrate a simplified method of forming an integrated circuit according to an embodiment of the present invention. These diagrams are merely examples, which should not unduly limit the scope of the claims herein. One of ordinary skill in the art would recognize many variations, modifications, and alternatives. As shown, the method begins providing a substrate 101. The substrate can be a silicon wafer, a multilayered structure, including silicon on insulator, and the like. The method includes forming an insulating layer ~~103~~ (not shown in Fig. 1: e.g., silicon dioxide, ~~florinated~~ fluorinated silicon oxide, black diamond a trade name by Applied Materials, Inc., SiLK a trade name by Dow chemical ~~and~~ or other dielectric materials) overlying the substrate. A dielectric layer 105 is formed overlying the insulating layer. The dielectric layer is patterned and metal material 107 fills the patterned dielectric material. A barrier metal layer may be formed between the metal fill material and the patterned dielectric material. Here, the metal material can be copper or the like and the patterned dielectric material can be silicon dioxide, ~~florinated~~ fluorinated silicon oxide, black diamond a trade name by Applied Materials, Inc., SiLK a trade name by Dow chemical and other dielectric materials. The barrier metal layer can be titanium, titanium nitride, tantalum, tantalum nitride, tungsten and its alloy, Mo, WNi and MoN. A planarizing method flattens or planarizes an upper surface of the metal and dielectric material layers. Of course, one of ordinary skill in the art would recognize many variations, alternatives, and modifications.

Please replace paragraph **[0023]** with the following amended paragraph:

[0023] Referring to Figure 2, each of the openings is filled with a metal layer 201, which ~~occupying~~ occupies substantially an entire region of each of the openings to form a plurality of metal structures. Each of the metal ~~structure~~ structures has a width and height. The method also planarizes ~~203~~ a surface of the metal layer 201. Preferably, the method uses similar techniques as those in a conventional dual damascene structure for copper interconnects or the like. As shown, the method forms the capacitor structure and interconnect structure using the same process steps at this point.